

IN THE CLAIMS:

Please accept the following amended claims:

1. (Currently Amended) ~~A MOSFET logic circuit for performing a logic OR operation comprising three transistors, first and second transistors of the three transistors forming a transmission gate outputting one signal, and wherein at least two input signals are provided to the first and second transistors and an output signal indicative of an OR operation performed on a first and second input signal of the at least two input signals is output from the MOSFET logic circuit.~~ OR logic circuit having a single logic gate for performing a logic OR operation comprising three transistors capable of receiving at least two OR input signals, and outputting a usable output signal indicative of an OR operation performed on first and second OR input signals of the at least two OR input signals;

a first of said three transistors being an pMOS transistor, a second of said three transistors being an nMOS transistor, and a third of said three transistors being a pull-up pMOS transistor, such that a transmission gate is formed at a junction of said pMOS transistor and said nMOS transistor;

wherein said first OR input signal is provided to said pMOS transistor and to said nMOS transistor, said second OR input signal is provided to the gate of said pMOS transistor, and the complement of said second OR input signal is provided to the gate of said pull-up pMOS transistor; and

wherein when said second OR input signal is high, said transmission gate is open, and when said second OR input signal is low, said transmission gate is closed.

2-6. (Canceled)

7. (Currently Amended) The MOSFET logic circuit as in claim 1, wherein when the second OR input signal has a logic LOW level the output of the MOSFET logic circuit is an output signal of the transmission gate.

8. (Currently Amended) The MOSFET logic circuit as in claim 1, ~~wherein a third transistor of the three transistors is a pull-up transistor, and~~ wherein when the second OR input signal has a logic HIGH level the output of the MOSFET logic circuit has a voltage level approximately equal to a drain of the third transistor, which pulls up the output signal from the transmission gate to a logic HIGH level.

9. (Previously Amended) The MOSFET logic circuit as in claim 1, wherein a delay of the MOSFET logic circuit is one of a delay of a transmission gate formed by first and second transistors of the three transistors, and a delay of a third transistor of the three transistors.